F F X

FAST FUNCTIONAL ACCELERATION

The IKOS RTL compiler enables SoC designers to realize the advantages of RTL verification with high-speed compilation and high-performance hardware-assisted solutions, turning weeks of RTL simulations into days or even hours.

HIGH-PERFORMANCE RTL COMPILER TECHNOLOGY TO ENABLE HARDWARE-ASSISTED RTL ACCELERATION OF VHDL OR VERILOG DESIGNS

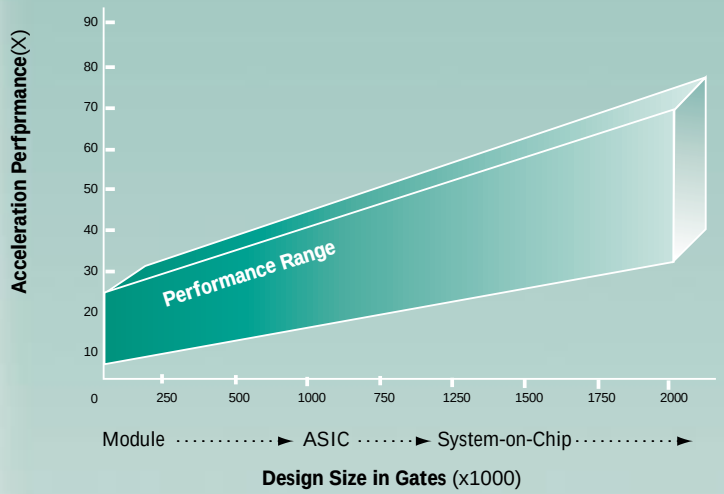
With system-on-chip (SoC) designs growing from 500,000 to multi-million gates, design engineers are facing rapidly expanding functional verification requirements. The IKOS RTL compiler is designed to provide a fast path to accelerate RTL simulation with IKOS hardware.

IKOS' unique RTL compiler technology consists of software programs that support high-performance Verilog and VHDL analyzers combined with a RTL compiler. This RTL software program is the key to the compiler technology, combining algorithms and data structure with gate count capacity to deliver compile times in the range of 50,000 simulation gates per minute.

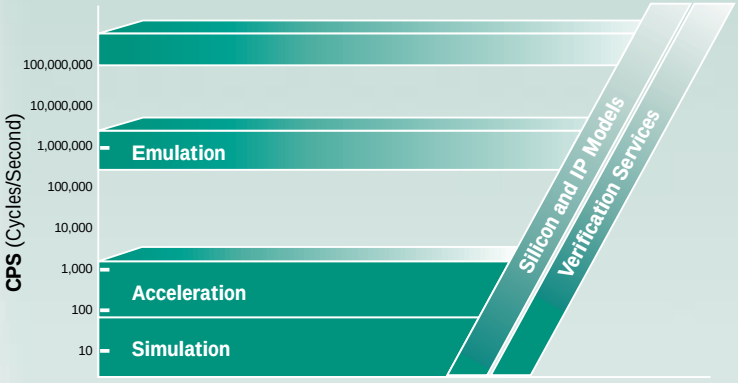
The RTL compiler is a breakthrough technology that allows design companies to leverage their current investments in IKOS NSIM hardware, utilizing this tool for RTL verification as well as gate level.

SIMULATION PERFORMANCE

The RTL compiler integrates efficiently with the IKOS NSIM hardware accelerator, allowing rapid verification development of RTL descriptions while maintaining the integrity of design signal names and hierarchy. The compiler enables RTL descriptions in VHDL and Verilog to be loaded directly onto the hardware accelerator and run at speeds higher than RTL software simulators running on workstations. For example, regression tests that would take two to three weeks on an RTL software simulator can be performed with the RTL compiler and NSIM hardware accelerator in a matter of days, or even as quickly as several hours, allowing multiple runs in one working day.



- Fast Verification Turnaround from Fast Compile and Accelerated Simulation
- Works for both Gemini Verilog and Voyager VHDL Design Flows
- Supports up to 16 Million Gate Designs
- Accelerated Performance and RTL Level Debug
- Direct Support for RTL IP Models
- No Simulation Libraries Required



"VOYAGER FFX GIVES A SIGNIFICANT BOOST IN OUR FUNCTIONAL VERIFICATION PRODUCTIVITY SINCE INTEGRATING THE ACCELERATOR AT THE RTL LEVEL DELIVERS 15X SIMULATION PERFORMANCE AND MUCH SHORTER COMPILE TIMES. FURTHERMORE, VOYAGER FFX IS COMPLEMENTARY TO OUR EXISTING FLOW AND MAKES ACCELERATION ACCESSIBLE EARLIER IN THE DESIGN CYCLE. IT'S THE IDEAL DEVELOPMENT TOOL TO SHORTEN OUR TIME TO MARKET FOR NEW SEMICONDUCTOR PRODUCTS WITH GATE COUNTS BIGGER THAN 300K, LIKE THE MUNICH 256F, OUR 256-CHANNEL HDLC CONTROLLER WITH INTEGRATED FRAMER."

Juergen Wolf
Data Communications Product Development Manager,
Infineon Technologies (formerly Siemens Microelectronics, Inc.)

TIME TO ACCELERATION

In addition to the performance enabled by hardware-assisted acceleration, the speed of the IKOS RTL compiler is on par with the fastest compiler technology used on the most popular compiled-code software simulators in the market.

When running RTL simulations without timing, primitive utilization is extremely efficient. Since there is no need for full-timing constraints that require a significant number of accelerator primitives, the equivalent RTL source can be mapped onto the hardware with better than a one-to-one primitive-to-gate ratio.

The RTL compiler has shown in recent benchmark studies to generate on average of 50,000 gates per minute. FFX also supports an incremental compile capability that allows fast hierarchical re-compiles at the module level. Because of the smaller resulting simulation image, FFX allows more efficient hardware utilization, which makes it practical to use hardware much earlier in the design process when frequent re-compiles are required.

MIXED-LEVEL COMPILATION

To create RTL descriptions that can be accelerated, the RTL compiler parses the mixed-level VHDL or Verilog design to identify the synthesizable sections of the design. The tool then compiles these sections into a netlist optimized for the high-performance NSIM hardware accelerator. This higher level RTL netlist is then processed, downloaded and simulated on the hardware accelerator. The design is partitioned to determine the portions of the source code that are RTL versus behavioral code. The portion that is purely behavioral and non-synthesizable will be left untouched and simulated on the software platform.

EASE OF USE

The IKOS RTL compiler is easily integrated into the design process flow. The automatic compilation allows the designer to go straight to the NSIM hardware accelerator and run very fast RTL descriptions without going through a synthesis step. Typically, the synthesis step can inadvertently change the signal names from the original design description and make it more difficult to debug the system when comparing gates to RTL. This problem is avoided by mapping directly to hardware accelerator primitives and maintaining both signal name integrity and design hierarchy.

THE NSIM HARDWARE ACCELERATOR

Hardware accelerators are custom hardware dedicated to simulation through high-speed RAM and proprietary ASIC designs architected for parallel, pipelined operation. The NSIM hardware accelerator uses high-speed static RAM to map functional gates to "lookup tables" in memory. The large amount of memory allows the structure to be mapped primitive-by-primitive into what amounts to equivalent gates. This specialized hardware performs like many workstations running in parallel, with the simulation residing in memory on the accelerator instead of in the workstation's local memory image.

When running RTL simulations, these primitives are used to map directly to the NSIM hardware accelerator. No timing accurate library is needed with the RTL compiler, so the mapping can be optimized for speed rather than timing accuracy. If accurate timing is required, the same accelerator can be used for full-timing gate-level simulations in conjunction with IKOS Voyager or Gemini products. NSIM's dual capability of RTL and gate-level acceleration maximizes the designer's investment in IKOS tools. The RTL compiler speed combined with the proven technology of hardware acceleration provide the performance gain needed for verifying increasingly complex SoC designs.

PERFORMANCE CHART

Design Size in gates	Compile Time in gates/minute	Performance Increase*
29,300	12,721	5.63X
35,000	50,000	12.38X
74,000	174,803	15X
345,000	N/A	23X
900,000	22,122	13.5X
2,000,000	28,513	75X

*Over leading software VHDL simulators.

SPECIFICATIONS

Architecture	Optimized RTL for NSIM Hardware
Platform Support	Sun Solaris and HP-UX support
Recommended Workstation Memory	256 MByte
Licensing	Flex-LM Licensing
Installation	Media CD-ROM

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