A R E S

PERSONAL RTL ACCELERATION

The ARES RTL Accelerator provides an integrated and accelerated RTL verification solution leveraging high-performance, low-cost hardware for desktop applications, compacting weeks of RTL simulations into hours.

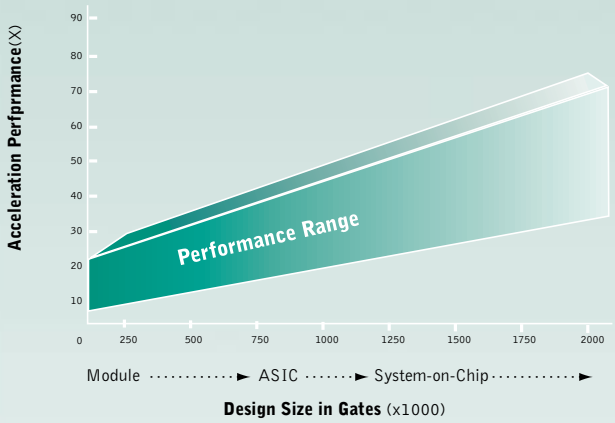
HIGH-PERFORMANCE, LOW-COST DESKTOP SOLUTION FOR RTL DESIGN VERIFICATION COMBINING PROVEN ACCELERATOR TECHNOLOGY WITH UNIQUE RTL COMPILER

The new ARES RTL Accelerator features specially engineered acceleration technology packaged with IKOS software to deliver the highest performance available for functional simulations. Designed as a solution to RTL performance challenges in the face of increasing design complexity, ARES provides a personal desktop accelerator — an affordable system for each engineer's desk — with the lowest cost per gate available anywhere.

ARES is the third offering in IKOS' series of innovative fast-functional verification products, which include Voyager FFX for RTL verification of VHDL designs and Gemini FFX for Verilog designs. ARES supports mixed-level acceleration at the register transfer level (RTL) for IKOS Voyager and Gemini verification environments, with all the modeling capacity and the highest RTL simulation speed attainable with today's technology.

ARES delivers 7X to 25X performance over leading software RTL simulators and delivers compile times in the range of 50,000 gates per minute with the latest RTL compiler from IKOS. The result is fast time-to-acceleration, and with added incremental compile capability, even faster debug turns. This potent combination of innovative compiler software and enhanced hardware accelerator technology provides a productivity boost to reduce the design cycle dramatically — not only earlier in the process, but where it counts the most, during the functional verification phase.

- Fast Verification Turnaround from Fast Compile and Accelerated RTL Simulation
- Performance Range 7-25X Over Software-Only Simulation
- Low-Cost Package Includes Software for Verilog and VHDL Designs
- Quick Design Turns with Incremental Compile
- Accelerated Performance and RTL Level Debug
- Direct Support for RTL IP Models
- Web-Based Memory Generation Tool



"RTL simulation has become the dominant verification challenge in our design flow, especially as our design complexity increases. ARES provides us with the robust fast-functional performance we need at an affordable price so we can readily incorporate it into our design verification environment."

Perry Farazi
Director of VLSI Design, Tellabs Operations, Inc.

ARES

INDUSTRY LEADING PRICE/PERFORMANCE

The state-of-the-art ARES technology has enabled IKOS to offer industry-leading price/performance for RTL acceleration. With a cost per gate as low as 3 cents due to the highly-efficient RTL compiler, IKOS has made acceleration affordable for every desktop. No other verification system can match the power and reliability for an individual acceleration system.

HIGH-PERFORMANCE RTL ACCELERATOR

The ARES system is based on proven accelerator technology modified with a new ARES system board developed to handle designs reaching 1 to 3 million gates at the RTL design level. ARES uses parallel, pipelined architecture to match the power and performance of an entire team of workstations.

The IKOS RTL compiler software integrates efficiently with the ARES hardware, allowing RTL descriptions to be loaded directly onto the accelerator. By mapping the RTL directly to hardware accelerator primitives, the user bypasses a synthesis step, and maintains the integrity of signal names and design hierarchy for more effective debug.

The ARES system is a mixed-level platform that supports behavioral testbenches running on the workstation concurrent with RTL simulations running on the hardware accelerator, therefore eliminating the design restrictions that other RTL cycle-based simulators place on testbench development. ARES accelerates the synthesizable subset of the RTL source code in conjunction with all memories, achieving as much as 1,000 simulated cycles per second — much higher than RTL software simulators running on workstations.

The performance improves as design sizes increase because of the ARES parallel processing technology. Benchmark designs of 1M+ gates have realized a 75X improvement over leading RTL software simulators. With the power of ARES, regression tests that would take weeks of software simulations can now take hours.

FAST RTL COMPILATIONS

ARES is supported by an extremely fast RTL synthesis engine employing state-of-the-art algorithms and data structures to deliver compile times in the range of 50,000 simulation gates per minute. The speed of the IKOS RTL compiler is on par with the fastest compiler technology used on the most popular compiled-code software simulators in the market, and it is 10X to 50X faster than a minimum synthesis to gates step.

The RTL synthesis tool is combined with high-performance built-in analyzers for both VHDL and Verilog, and has been further optimized to support the ARES RTL system through tight integration, allowing rapid RTL verification.

TIME TO ACCELERATION

No simulation target library is needed for RTL acceleration, enabling quick download and easy startup for reduced time to acceleration. When running RTL simulations without timing, primitive utilization is extremely efficient, and the equivalent RTL source can be mapped onto the hardware with as high as two-to-one primitive-to-user gate ratio.

DESIGN TURNAROUND

ARES supports an incremental compile capability so fast design turnaround can take place at a fraction of the original compile time. Fast hierarchical recompiles at the module level allow more efficient hardware utilization much earlier in the design process when frequent recompiles are required.

MEMORY ACCELERATION

ARES also features on-board memory capacity for memory modeling and integration of verification IP models, such as the Rambus general-purpose high-performance memory device and the ARM core, to help verify these complex SoC designs. Fast memory generation is also enabled through IKOS' web-based functional memory generation tool.

SPECIFICATIONS

	Base System	Upgraded System
Processors	7	15
Primitive Capacity	1.6M	3.6M
Memory (LMM)	64 Mbytes	64 Mbytes
Memory (SMM)	4 Mbits	8 Mbits
Dimensions (h, w, d inches)	16x5x20	16x5x20
(h, w, d mm)	406x127x508	406x127x508
Power	500W, 100-240 VAC, 1Ø	500W, 100-240 VAC, 1Ø
Cooling	Forced Air	Forced Air

ARES

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